averant

Solidify™

Static Functional Verification

Features
- High-performance engines
- Source-code debugging
- Hierarchical verification
- Memory model generation
- Property code coverage
- Automatic design checks

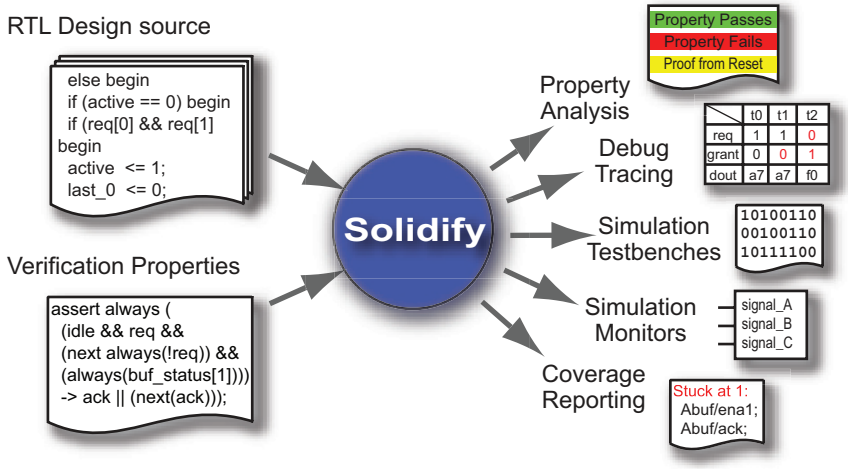
Languages
- Verilog / VHDL
- SVA, PSL, OVA, OVL

Outputs
- Property analysis results
- Debug tracing & waveforms
- Testbench generation
- Simulation monitor generation
- Coverage reporting

Overview

Static functional verification is a unique form of analysis applied to RTL design descriptions. The strength of this analysis is that it is exhaustive by nature, and quickly uncovers hidden design flaws and corner cases.

Solidify is the state of the art in static functional verification. The underlying technology is very mature, having been employed on countless production designs. Solidify is feature-rich, powerful, and flexible, allows use by both designers and verification engineers, and adapts easily to any environment. It offers capabilities for both novice and expert users, and interfaces to other programs such as simulators and debuggers.



Push-button Capabilities

Solidify includes a rich set of automatic checks, making it easy to reap the benefits of formal verification. These can be used on any design, and require no knowledge of formal verification techniques or languages:

- Deadlock / Livelock
- Case pragma
- Reset propagation
- Dead code
- Contention
- Data stability
- Clock crossing
- Array bounds
- Gray code check

Powerful Tools

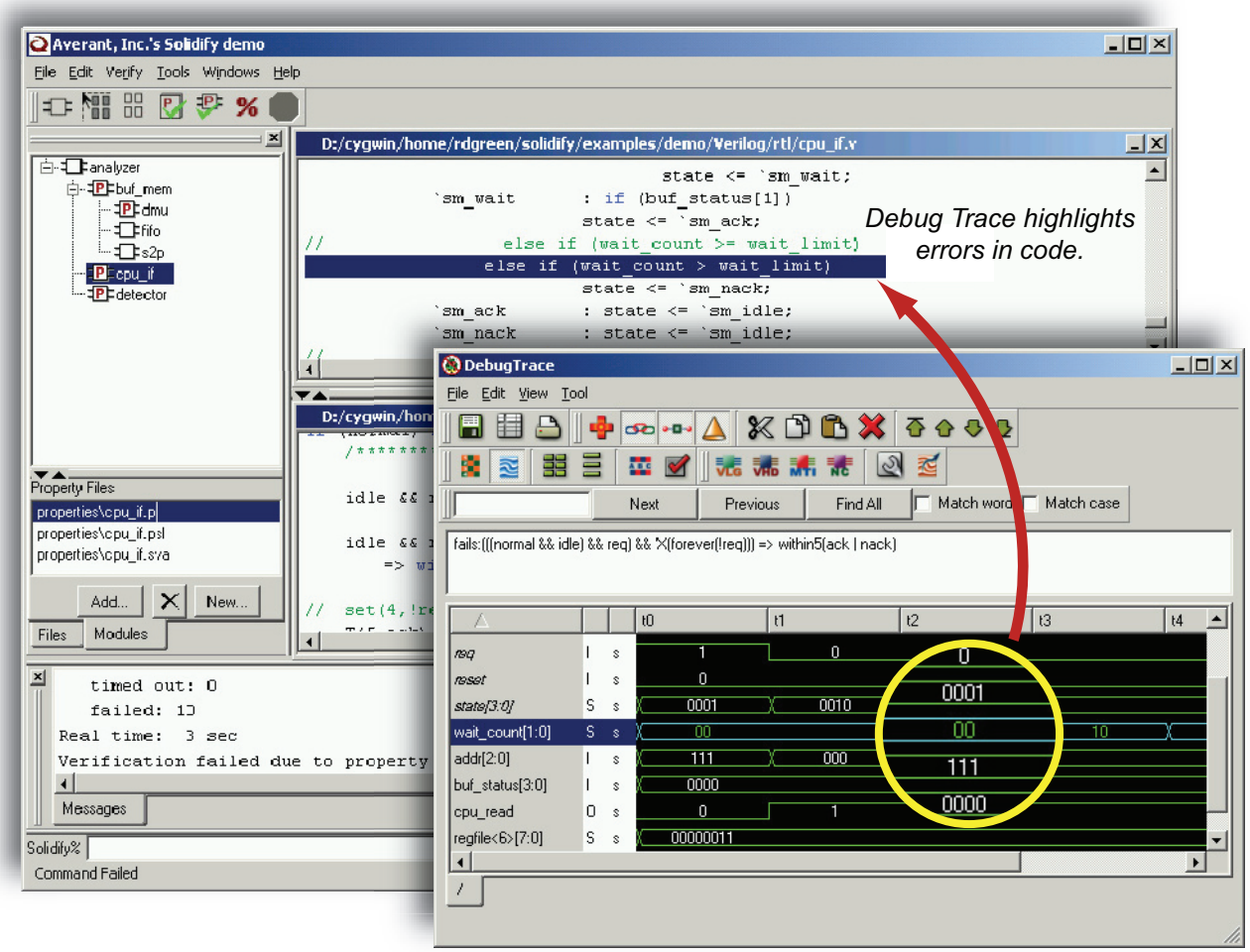
Power-users will appreciate Solidify's ability to input properties written in PSL, SVA, and OVL. Solidify has the unique ability to write-out properties in any of those languages, helping to preserve verification IP value if migrating assertion languages. Solidify also includes a host of advanced capabilities such as constraints handling, assumption processing, hierarchical verification, and supports specific protocol checking verification components.

Patented Technology

Solidify includes Averant's unique, patented code coverage capability. This technology allows users to check the property set for a given design to ensure at least minimal coverage of the design. Property coverage can also be used to optimize regression suites for both static and dynamic verification.

Flexible Environment

Solidify offers a rich graphical environment with source-code debugging capabilities. Solidify also supports Tcl-based programming for full batch-type execution.



Solid Benefits

Solidify provides designers and verification engineers with the methodology and technology to use static functional verification to greatly enhance existing verification flows. The concise and comprehensive nature of properties make a static verification environment easier to develop than for dynamic verification. And the exhaustive nature of formal verification makes it easy to catch both simple bugs earlier in the design cycle as well as catching subtle bugs and corner cases.

These factors make Solidify a powerful tool to help increase design quality, speed verification, and reduce costs.

Averant, Inc.
22320 Foothill Blvd., suite 360
Hayward, CA 94541

averant

Tel: 510-881-8881
Fax: 510-881-8886
www.averant.com